APPLICATION NOTE

STPC Client Motherboard Start-Up

by T. Seigneurie & M.Tabet

1. Overview.

This document provides detailed information regarding the way to start-up a new STPC Client Motherboard. This document intends to eliminate basic hardware problem which will prevents the STPC Client from start working.

The following "procedure" is a step by step one. Therefore in this document we assume that you have followed this step by step way and that you do not "jump" to a specific item but follow the complete process.

This document is intended to support the following device:

STPC Client

For additional information on the STPC Client specifications, please refer to the STPC Client Databook. Information in this document is subject to change without notification.

STMicroelectronics values your feedback. Please send it and any recommendations you may have regarding this document to *stpc.support@st.com* with the subject line "AN1080".

2. STPC Client Checking.

Four main conditions can prevent an STPC Client Motherboard from working:

- Power Supply
- STPC Configuration
- Clock Circuitry
- Reset Circuitry

2.1 Power Supply.

It is an obvious statement that an defectif or incorrect Power Supply may generate unreliable behavior by the STPC Client. Nevertheless, the STPC has several different Power domains that should be checked when starting-up a new STPC motherboard.

Before powering-up your STPC Client, please verify that the Power Pins are correlctly connected according to the following table:

TABLE 1. STPC Client Power Pins Connections

Pin Name	Pin Function	Pin Number	Required Voltage
VDD	Logic PS	B14, C9, D6, D11, D16, D21, F4, F23, G1, K23, L4, L23, P2, T4, T23, T26, AA4, AA23, AB23, AC6, AC11, AC16, AC21	3.3V+/-0.3
VDD5	5VI/O tol.	A16, B12, B9, D18	5V +/- 0.5
VDDE	Logic PS*	AF13, AD19	3.3V+/-0.3
VDD_DAC1/2	DAC PS*	AC7, AF4	3.3V+/-0.3
VDD_GCLK_PLL	GCLK_PLL PS*	WA	3.3V+/-0.3
VDD_DCLK_PLL	DCLK_PLL PS*	AB1	3.3V+/-0.3
VDD_HCLK_PLL	HCLK_PLL PS*	F26	3.3V+/-0.3
VDD_DEVCLK_PLL	DEVCLK_PLL PS*	G24	3.3V+/-0.3

* PS means Power Supply.

Ground connections are also important for the chip behavior. Please verify that the Ground Pins are correctly connected according to the following table.

TABLE 2. STPC Client Ground Pins Connections

Pin Name	Pin Function	Pin Number
VSS	Logic GND	A1, A2, A26, B2, B25, B26
		C3, C24, D4, D9, D14, D19
		D23, H4, J23, L11:16,
		M11:16, N4, N11:16,
		P11:16, P23, R11:16,
		T11:16, V4, W23, AC4,
		AC8, AC13, AC18, AC23,
		AD3, AD24, AE1, AE2,
		AE25, AF1, AF25, AF26
VSS_DAC1/2	DAC GND	AE7, AF7
VSS_PLL	All PLLs GND	E25, E26

2.2 STPC Client Configuration

STPC Client has been designed in a way to allow configurations for test purpose that differs from the functional configuration. Assuming that you have checked that the STPC is properly powered (see 2.1), the next step consists in checking that the STPC Client Configuration is correct.

STPC Client is configured at the rising edge of PWERGD (?or SYSRESET).

TABLE 3. STPC Client Configuration

Pin Name	Pin Number	Expected Configuration	Notes (*)
ST0:3	B4, D5, A4, C5	4.7K Pup	STPC as STPC
CLKDEL0	C7	4.7K Pdn	For DX2 Mode
CLKDEL1	B5	4.7K Pup	For DX2 Mode
CLKDEL2	A5	4.7K Pdn	For DX2 Mode
MD31	G26	4.7K Pdn	HCLK Skew
MD32	AD22	4.7K Pup	HCLK Skew
MD33	AD23	4.7K Pup	HCLK Skew
MD34	AE26	4.7K Pdn	HCLK Skew
MD35	AD26	4.7K Pup	HCLK Skew
MD16	U24	4.7K Pup	Test Bus Off
MD17	R26	4.7K Pup	PCICLK=HCLK/2
MD19	P26	4.7K Pdn	Int. PLL for GCLK
MD20	N25	4.7K Pup	
MD21	N26	4.7K Pup	
MD22	M25	4.7K Pup	
MD23	M26	4.7K Pup	

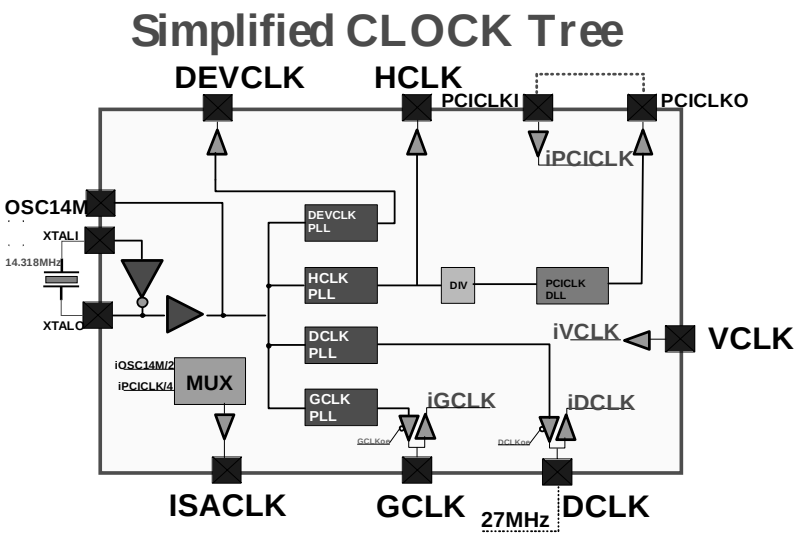
MD24:MD26 must have 4.7Pup or 4.7Pdn according to the frequency that has been selected for HCLK.

(*) Notes are often meaningless for the STPC Client users

2.3 Clock Circuitry

STPC Client has a complex Clock Circuitry that allows the generation of all external frequencies from a single 14.318MHz Crystal Oscillator. This simplifies the board design but means also that a default in the clock input can generate a bad behavior of the STPC Client. (See below the STPC Internal Clock Tree).

2.4 Clock



Assuming that you have checked that the STPC is properly powered (see 2.1) and properly configured (see 2.2), the next step consists in checking the Clock circuitry. For this please check it in the following order:

TABLE 4. STPC Client Clocks

Pin Name	Pin Number	Expected Clock Value	Possible cause of problem
XTALO	AE16	14.318MHz	Bad Osc. short on BD*
OSC14M	C6	14.318MHz	Bad conf ST[0..6]
DEV_CLK	F25	24MHz	short on BD*
HCLK	G23	66MHz (dep. Sel)	sh. on BDx*
GCLK2X	AC5	yyMHz	sh. on BD*/bad Conf MDxx
DCLK	AD5	zzMHz	sh. on BD*/bad DCLKDIR
PCI_CLKO	D25	HCLK/2or 3(dep. Sel)	sh. on BD*
PCI_CLKI	F24	PCI_CLKO	Mis with PCI_CLKO

BD means Board.

2.5 Reset Circuitry.

Reset of the STPC is used internally to latched configuration strap values on the MD bus. Therefore a bad or missing Reset signal can generate an unexpected behavior of the STPC Client.

Assuming that you have checked that the STPC is properly powered (see 2.1), properly configured (see 2.2) and has the proper clocks, the next step consists in checking the Reset Circuitry. For that please check it in the following order:

TABLE 5. STPC Client Reset Circuitry

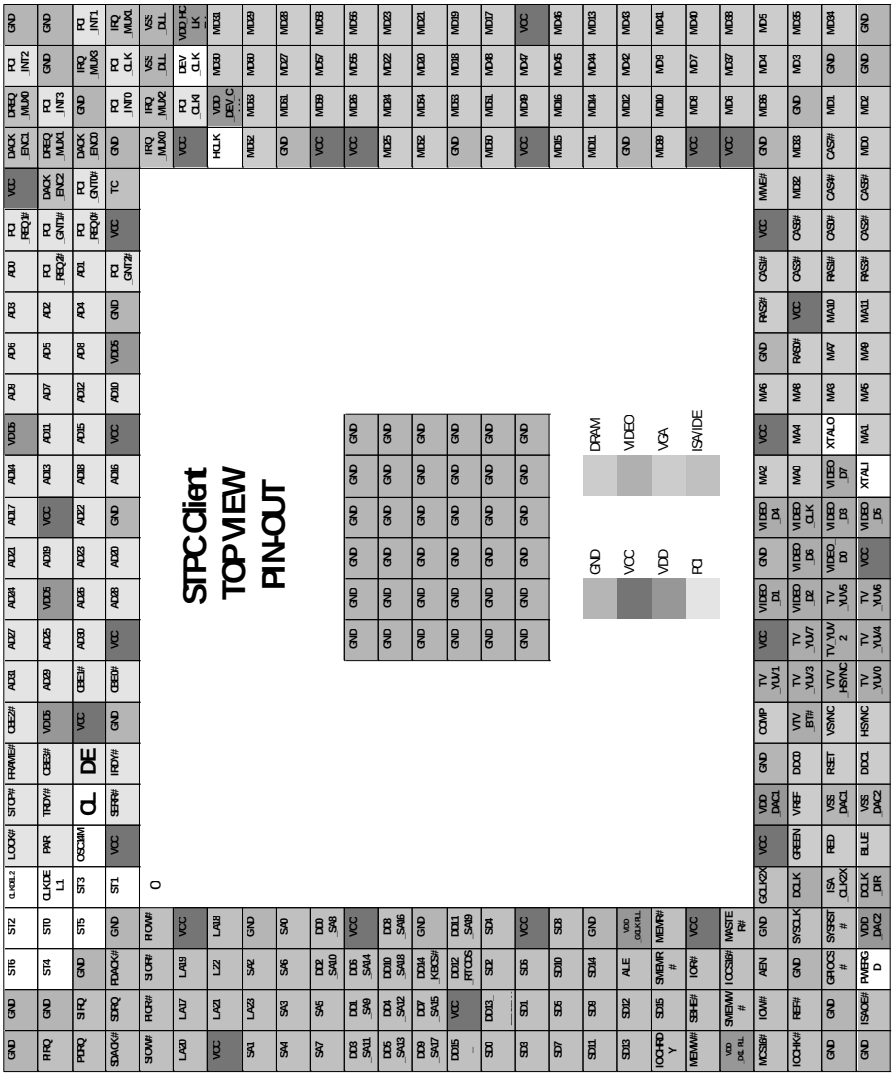
Pin Name	Pin Number	Expected Behavior	Possible cause of problem
PWERGD	AF3	High (TTL level) when Power is OK. Low (TTL level) when Power is Not OK or reset button is pressed	Sh. on BD/Miss. Connect to PS or reset button
SYSRESET0x	AE4	High when PWERGD is high sh.on BD. Low when PWERGD is low.	

Once the former steps has been checked, the STPC Client by itself should be working fine. Additional problems can come from the board design itself or the SIO that has been selected.

When the STPC is working fine the signal RMRTCCS (P1) is activated after Power On and as long as the ROMBIOS Flash is accessed.

The SIO configuration can also create problems during the boot phase, therefore it is important to refer to the relevant documentation to check that it has been properly configured.

3. STPC Client Pinout



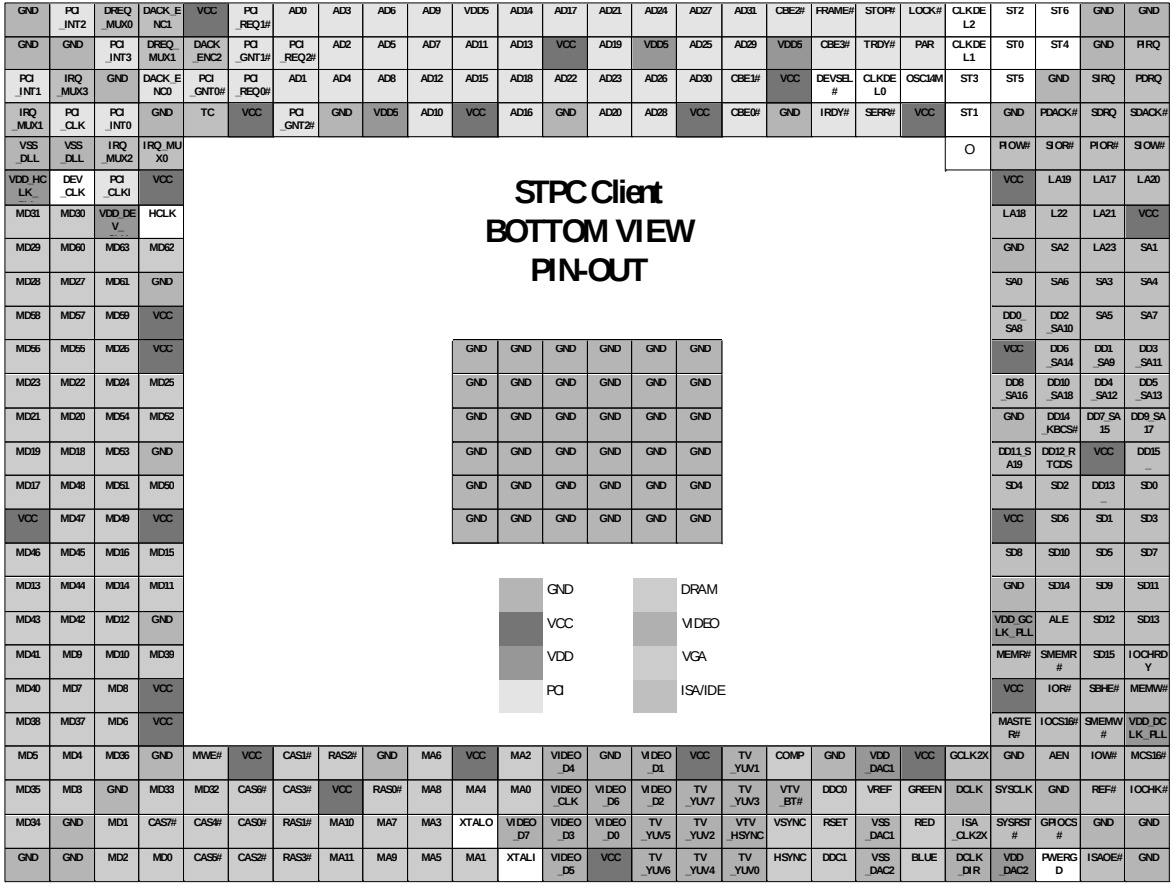
STPC Client TOP VIEW PIN-OUT

GND	GND	ST6	ST2	CLKDEL2	LOCK#	STOP#	FRAME#	CBE2#	AD31	AD27	AD24	AD21	AD17	AD14	VDD5	AD9	AD6	AD3	AD0	PCI_REQ1#	VCC	DACK_ENC1	DREQ_MUX0	PCI_INT2	GND
PIRQ	GND	ST4	ST0	CLKDEL1	PAR	TRDY#	CBE3#	VDD5	AD29	AD25	VDD5	AD19	VCC	AD13	AD11	AD7	AD5	AD2	PCI_REQ2#	PCI_GNT1#	DACK_ENC2	DREQ_MUX1	PCI_INT3	GND	GND
PDRQ	SIRQ	GND	ST5	ST3	OSC14M	CLKDEL0	DEVSEL#	VCC	CBE1#	AD30	AD26	AD23	AD22	AD18	AD15	AD12	AD8	AD4	AD1	PCI_REQ0#	PCI_GNT0#	DACK_ENC0	GND	IRQ_MUX3	PCI_INT1
SDACK#	SDRQ	PDACK#	GND	ST1	VCC	SERR#	IRDY#	GND	CBE0#	VCC	AD28	AD20	GND	AD16	VCC	AD10	VDD5	GND	PCI_GNT2#	VCC	TC	GND	PCI_INT0	PCI_CLK	IRQ_MUX1
SIOW#	PIOR#	SIOR#	PIOW#	O																		IRQ_MUX0	IRQ_MUX2	VSS_DLL	VSS_DLL
LA20	LA17	LA19	VCC																			VCC	PCI_CLKI	DEV_CLK	VDD_HCLK
VCC	LA21	L22	LA18																			HCLK	VDD_DEV	MD30	MD31
SA1	LA23	SA2	GND																			MD62	MD63	MD60	MD29
SA4	SA3	SA6	SA0																			GND	MD61	MD27	MD28
SA7	SA5	DD2_SA10	DD0_SA8																			VCC	MD59	MD57	MD58
DD3_SA11	DD1_SA9	DD6_SA14	VCC																			VCC	MD26	MD55	MD56
DD5_SA13	DD4_SA12	DD10_SA18	DD8_SA16																			MD25	MD24	MD22	MD23
DD9_SA17	DD7_SA15	DD14_KBCS#	GND																			MD52	MD54	MD20	MD21
DD15_	VCC	DD12_RTCDS	DD11_SA19																			GND	MD53	MD18	MD19
SD0	DD13_	SD2	SD4																			MD50	MD51	MD48	MD17
SD3	SD1	SD6	VCC																			VCC	MD49	MD47	VCC
SD7	SD5	SD10	SD8																			MD15	MD16	MD45	MD46
SD11	SD9	SD14	GND																			MD11	MD14	MD44	MD13
SD13	SD12	ALE	VDD_GCLK																			GND	MD12	MD42	MD43
IOCHRDY	SD15	SMEMR#	MEMR#																			MD39	MD10	MD9	MD41
MEMW#	SBHE#	IOR#	VCC																			VCC	MD8	MD7	MD40
VDD_DCLK	SMEMW#	IOCS16#	MASTER#																			VCC	MD6	MD37	MD38
MCS16#	IOW#	AEN	GND	GCLK2X	VCC	VDD_DAC1	GND	COMP	TV_YUV1	VCC	VIDEO_D1	GND	VIDEO_D4	MA2	VCC	MA6	GND	RAS2#	CAS1#	VCC	MWE#	GND	MD36	MD4	MD5
IOCHK#	REF#	GND	SYSCLK	DCLK	GREEN	VREF	DDC0	VTV_BT#	TV_YUV3	TV_YUV7	VIDEO_D2	VIDEO_D6	VIDEO_CLK	MA0	MA4	MA8	RAS0#	VCC	CAS3#	CAS6#	MD32	MD33	GND	MD3	MD35
GND	GND	GROCS#	SYSRST#	ISA_CLK2X	RED	VSS_DAC1	RSET	VSYNC	VTV_HSYNC	TV_YUV2	TV_YUV5	VIDEO_D0	VIDEO_D3	VIDEO_D7	XTALO	MA3	MA7	MA10	RAS1#	CAS0#	CAS4#	CAS7#	MD1	GND	MD34
GND	ISAOE#	PWERGD	VDD_DAC2	DCLK_DIR	BLUE	VSS_DAC2	DDC1	HSYNC	TV_YUV0	TV_YUV4	TV_YUV6	VCC	VIDEO_D5	XTALI	MA1	MA5	MA9	MA11	RAS3#	CAS2#	CAS5#	MD0	MD2	GND	GND

A1/1	A2/27	A3/53	A4/79	A5/ 105	A6/ 113	A7/ 121	A8/ 129	A9/ 137	A10/ 145	A11/ 153	A12/ 167	A13/ 181	A14/ 195	A15/ 209	A16/ 223	A17/ 237	A18/ 245	A19/ 253	A20/ 261	A21/ 269	A22/ 277	A23/ 285	A24/ 311	A25/ 337	A26/ 363
B1/2	B2/28	B3/54	B4/80	B5/ 106	B6/ 114	B7/ 122	B8/ 130	B9/ 138	B10/ 146	B11/ 154	B12/ 168	B13/ 182	B14/ 196	B15/ 210	B16/ 224	B17/ 238	B18/ 246	B19/ 254	B20/ 262	B21/ 270	B22/ 278	B23/ 286	B24/ 312	B25/ 338	B26/ 364
C1/3	C2/29	C3/55	C4/81	C5/ 107	C6/ 115	C7/ 123	C9/ 131	C9/ 139	C10/ 147	C11/ 155	C12/ 169	C13/ 183	C14/ 197	C15/ 211	C16/ 225	C17/ 239	C18/ 247	C19/ 255	C20/ 263	C21/ 271	C22/ 279	C23/ 287	C24/ 313	C25/ 339	C26/ 365
D1/4	D2/30	D3/56	D4/82	D5/ 108	D6/ 116	D7/ 124	D8/ 132	D9/ 140	D10/ 148	D11/ 156	D12/ 170	D13/ 184	D14/ 198	D15/ 212	D16/ 226	D17/ 240	D18/ 248	D19/ 256	D20/ 264	D21/ 272	D22/ 280	D23/ 288	D24/ 314	D25/ 340	D26/ 366
E1/5	E2/31	E3/57	E4/83																			E23/ 289	E24/ 315	E25/ 341	E26/ 367
F1/6	F2/32	F3/58	F4/84																			F23/ 290	F24/ 316	F25/ 342	F26/ 368
G1/7	G2/33	G3/59	G4/85																			G23/ 291	G24/ 317	G25/ 343	G26/ 369
H1/8	H2/34	H3/60	H4/86																			H23/ 292	H24/ 318	H25/ 344	H26/ 370
J1/9	J2/35	J3/61	J4/87																			J23/ 293	J24/ 319	J25/ 345	J26/ 371
K1/10	K2/36	K3/62	K4/88																			K23/ 294	K24/ 320	K25/ 346	K26/ 372
L1/11	L2/37	L3/63	L4/89																			L23/ 295	L24/ 321	L25/ 347	L26/ 373
M1/12	M2/38	M3/64	M4/90																			M23/ 296	M24/ 322	M25/ 348	M26/ 374
N1/13	N2/39	N3/65	N4/91																			N23/ 297	N24/ 323	N25/ 349	N26/ 375
P1/14	P2/40	P3/66	P4/92																			P23/ 298	P24/ 324	P25/ 350	P26/ 376
R1/15	R2/41	R3/67	R4/93																			R23/ 299	R24/ 325	R25/ 351	R26/ 377
T1/16	T2/42	T3/68	T4/94																			T23/ 300	T24/ 326	T25/ 352	T26/ 378
U1/17	U2/43	U3/69	U4/95																			U23/ 301	U24/ 327	U25/ 353	U26/ 379
V1/18	V2/44	V3/70	V4/96																			V23/ 302	V24/ 328	V25/ 354	V26/ 380
W1/19	W2/45	W3/71	W4/97																			W23/ 303	W24/ 329	W25/ 355	W26/ 381
Y1/20	Y2/46	Y3/72	Y4/98																			Y23/ 304	Y24/ 330	Y25/ 356	Y26/ 382
AA1/21	AA2/47	AA3/73	AA4/99																			AA23/ 305	AA24/ 331	AA25/ 357	AA26/ 383
AB1/22	AB2/48	AB3/74	AB4/ 100																			AB23/ 306	AB24/ 332	AB25/ 358	AB26/ 384
AC1/23	AC2/49	AC3/75	AC4/ 101	AC5/ 109	AC6/ 117	AC7/ 125	AC8/ 133	AC9/ 141	AC10/ 149	AC11/ 163	AC12/ 177	AC13/ 191	AC14/ 205	AC15/ 219	AC16/ 233	AC17/ 241	AC18/ 249	AC19/ 257	AC20/ 265	AC21/ 273	AC22/ 281	AC23/ 307	AC24/ 333	AC25/ 359	AC26/ 385
AD1/24	AD2/50	AD3/76	AD4/ 102	AD5/ 110	AD6/ 118	AD7/ 126	AD8/ 134	AD9/ 142	AD10/ 150	AD11/ 164	AD12/ 178	AD13/ 192	AD14/ 206	AD15/ 220	AD16/ 234	AD17/ 242	AD18/ 250	AD19/ 258	AD20/ 266	AD21/ 274	AD22/ 282	AD23/ 308	AD24/33 4	AD25/36 0	AD26/38 6
AE1/25	AE2/51	AE3/77	AE4/ 103	AE5/ 111	AE6/119	AE7/ 127	AE8/ 135	AE9/ 143	AE10/ 151	AE11/ 165	AE12/ 179	AE13/ 193	AE14/ 207	AE15/ 221	AE16/ 235	AE17/ 243	AE18/ 251	AE19/ 259	AE20/ 267	AE21/ 275	AE22/ 283	AE23/ 309	AE24/ 335	AE25/ 361	AE26/ 387
AF1/26	AF2/52	AF3/78	AF4/ 104	AF5/ 112	AF6/ 120	AF7/ 128	AF8/ 136	AF9/ 144	AF10/ 152	AF11/ 166	AF12/ 180	AF13/ 194	AF14/ 208	AF15/ 222	AF16/ 236	AF17/ 244	AF18/ 252	AF19/ 260	AF20/ 268	AF21/ 276	AF22/ 284	AF23/ 310	AF24/ 336	AF25/ 362	AF26/ 388

STPC Client
TOP VIEW
BGA-pin/Orcad-pin Correspondence

L11/ 157	L12/ 171	L13/ 185	L14/ 199	L15/213	L16/ 227
M11/ 158	M12/ 172	M13/ 186	M14/ 200	M15/214	M16/ 228
N11/ 159	N12/ 173	N13/ 187	N14/ 201	N15/215	N16/ 229
P11/ 160	P12/ 174	P13/ 188	P14/ 202	P15/216	P16/ 230
R11/ 161	R12/ 175	R13/ 189	R14/ 203	R15/217	R16/ 231
T11/ 162	T12/ 176	T13/ 190	T14/ 204	T15/218	T16/ 232


STPC Client
BOTTOM VIEW
PIN-OUT
GND
VCC
VDD
PCI
DRAM
VIDEO
VGA
ISA/IDE

4. Technical Support

STMicroelectronics is on the Internet with a worldwide web (WWW) site on which product presentation, technical literature as well as product support information can be found.

A dedicated STPC section is available providing up to date hardware documentation and software tools.

The Web and e-mail addresses are:

WWW **:** ***http://www.st.com/stpc***

e-mail : ***stpc.support@st.com***

5. Update History for Application Note AN 1080

The following changes have been made to the Application Note AN 1080 from Revision 1.0 to Release 1.1.

Page	Section	Change	Text
3	2.2	Replaced	Cell MD31 Expected Configuration from "~~4.7KPup~~" to "4.7KPdn"
3	2.2	Replaced	Cell MD32 Expected Configuration from "~~4.7KPdn~~" to "4.7KPup"
3	2.2	Replaced	Cell MD34 Expected Configuration from "~~4.7KPup~~" to "4.7KPdn"
3	2.2	Replaced	Cell MD35 Expected Configuration from "~~4.7KPdn~~" to "4.7KPup"
3	2.2	Replaced	Cell MD19 Expected Configuration from "~~4.7KPdn~~" to "4.7KPup"